REMARKS

The Office Action mailed March 29, 2001, has been received and reviewed. Claims 1 through 99 are currently pending in the application. Claims 1 through 28 stand rejected. Claims 29 through 99 have been withdrawn from consideration as being drawn to a non-elected invention. Applicant has cancelled claims 29-99. New claims 100 through 129 have been added. Applicant has amended claims 1, 11 and 16, and respectfully requests reconsideration of the application as amended herein.

Claim Objections

Claims 11 and 16 were objected to because of writing informalities.

Claim 11 was amended to correct the typographical error and recite that the claim is dependent from claim 1. Reconsideration of the objection is requested.

Claim 16 was amended to correct the error "on the at least one sidewall" and, as amended, recites "on at least one sidewall of said at least one sidewall." Applicant requests reconsideration of the objection.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,825,609 to Andricacos et al.

Claims 1 through 7, 10 through 12, and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Andricacos et al. (U.S. Patent No. 5,825,609). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Andricacos discloses a compound electrode stack capacitor. By way of contrast, claim 1, as amended, recites a metallization structure for a semiconductor device, comprising a substrate comprising a substantially planar upper surface and a conductive line for transmitting a signal laterally

across said substrate, said conductive line comprising a metal layer defining a pattern on a portion of the substrate upper surface, a conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said conducting layer having substantially aligned sidewalls and metal spacers flanking the sidewalls of the conducting layer and metal layer.

Applicant respectfully submits that independent claim 1, as amended, is not anticipated by Andricacos because Andricacos fails to disclose a conductive line for transmitting a signal laterally across a substrate. Further, Andricacos fails to disclose a conductive line comprising a metal layer defining a pattern on a portion of the substrate upper surface, a conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said conducting layer having substantially aligned sidewalls and metal spacers flanking the sidewalls of the conducting layer and metal layer. Instead, Andricacos merely discloses a storage element comprising a stack electrode.

Further, applicant respectfully submits that reliance on Andricacos is misplaced. The structure in Andricacos is for conducting *from an underlying* structure. (*See*, Andricacos, FIGs. 1a-14). By way of contrast, applicant's structure conducts *across* a substrate. Additionally, FIG. 5 of Andricacos appears to be an intermediate structure that is later capped with a plate electrode and another dielectric layer. (Andricacos, FIG. 10). As Andricacos is directed toward a semiconductor memory device including a compound electrode stack, applicant submits that Andricacos lacks any suggestion to build a conductive line as claimed in independent claim 1.

As the cited reference fails to teach every element of the presently claimed invention, applicant submits that independent claim 1 is not anticipated by Andricacos.

Claims 2 through 15 are each distinguishable from Andricacos for the same reasons as independent claim 1.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,701,647 to Saenger et al.

Claims 16 through 19, 24, and 26 through 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Saenger et al. (U.S. Patent No. 5,701,647). Applicant respectfully traverses this rejection, as hereinafter set forth.

Saenger discloses an isolated sidewall capacitor having a compound plate electrode that can be used with high dielectric constant materials. (Saenger, col. 1, lines 24-27). By way of contrast, claim 16, as amended, recites a metallization structure for a semiconductor device, comprising a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate, a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture flanking said conductive line, a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture and a conductive layer substantially filling a remaining portion of the aperture.

Applicant respectfully submits that independent claim 16, as amended, is not anticipated by Saenger because Saenger fails to disclose every element of the presently claimed invention. Saenger does not disclose a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate. Instead, Saenger lacks any disclosure of a conductive line. Further, Saenger only discloses a conductive plug for vertical conducting and does not disclose a metal layer underlying a conductive line for transmitting a signal across a substrate. Similarly, Saenger does not disclose an aperture flanking a conductive line and merely discloses conductive *plugs* 6,8, for vertical conducting. Saenger teaches away from a metal spacer abutting at least one sidewall. (Saenger, col. 4, lines 42-47). Additionally, Saenger does not disclose a conductive layer substantially filling a remaining portion of the aperture. Instead, Saenger discloses a filler 34 above a conductive layer 32 in an opening 26.

Further, applicant respectfully submits that reliance on Saenger is misplaced. The structure in Saenger is for conducting *from an underlying* structure. (*See*, Saenger, FIGs. 5A-5I). By way of contrast, applicant's structure is for conducting *across* a structure. As Saenger is directed toward a method of making an isolated sidewall capacitor having a compound plate electrode, applicant submits that Saenger lacks any suggestion to build a conductive line as claimed in independent claim 16.

Claims 15 through 28 are each distinguishable from Saenger for the same reasons as claim 16.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,825,609 to Andricacos et al.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Andricacos et al. (U.S. Patent No. 5,825,609). Applicant respectfully traverses this rejection, as hereinafter set forth.

As stated above, Andricacos is directed toward a semiconductor memory device including a compound electrode stack and lacks any suggestion to build a conductive line as required by the presently claimed invention and thus fails to teach or suggest every limitation of the presently claimed invention. Further, the Federal Circuit has clearly indicated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *See, In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). The M.P.E.P. specifically upholds the finding of *In re Fine*, stating: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *See*, M.P.E.P. § 2143.03, (citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, as independent claim 1, from which claims 8 and 9 depend, is nonobvious in view of Andricacos, applicant submits that claims 8 and 9 are also nonobvious. Reconsideration of the rejection is respectfully requested.

Obviousness Rejection Based on U.S. Patent No. 5,825,609 to Andricacos et al., and Further in View of U.S. Patent No. 6,046,502 to Matsuno

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Andricacos et al. (U.S. Patent No. 5,825,609), as applied to claims 1 through 7, 10 through 12, and 15 above, and further in view of Matsuno (U.S. Patent No. 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

As stated above, Andricacos is directed toward a semiconductor memory device including a compound electrode stack and lacks any suggestion to build a conductive line as required by the presently claimed invention. Matsuno is directed toward a semiconductor device with improved adhesion between a titanium-based metal layer and an insulation film and fails to cure any of the deficiencies of Andricacos. Further, the Federal Circuit has clearly indicated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *See, In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). The M.P.E.P. specifically upholds the

finding of *In re Fine*, stating: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *See*, M.P.E.P. § 2143.03, (citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, as independent claim 1, from which claims 13 and 14 depend, is nonobvious in view of cited references, applicant submits that claims 13 and 14 are also nonobvious. Reconsideration of the rejection is respectfully requested.

Obviousness Rejection Based on U.S. Patent No. 5,701,647 to Saenger et al., and Further in View of U.S. Patent No. 5,825,609 to Andricacos et al.

Claims 20 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Saenger et al. (U.S. Patent No. 5,701,647), as applied to claims 16 through 19, 24, and 26 through 28 above, and further in view of Andricacos et al. (U.S. Patent No. 5,825,609). Applicant respectfully traverses this rejection, as hereinafter set forth.

As stated above, neither Saenger nor Andricacos include any teaching or suggestion to build a conductive line as required by the presently claimed invention. Thus, the proposed combination of references fails to teach or suggest every limitation of the presently claimed invention. Further, the Federal Circuit has clearly indicated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *See*, *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). The M.P.E.P. specifically upholds the finding of *In re Fine*, stating: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *See*, M.P.E.P. § 2143.03, (citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, as independent claim 16, from which claims 20 and 23 depend, is nonobvious in view of cited references, applicant submits that claims 20 and 23 are also nonobvious. Reconsideration of the rejection is respectfully requested.

Obviousness Rejection Based on U.S. Patent No. 5,701,647 to Saenger et al., and Further in View of U.S. Patent No. 5,578,523 to Fiordalice et al.

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Saenger et al. (U.S. Patent No. 5,701,647), as applied to claims 16 through 19, 24, and 26 through 28 above,

and further in view of Fiordalice et al. (U.S. Patent No. 5,578,523). Applicant respectfully traverses this rejection, as hereinafter set forth.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *See* M.P.E.P. 706.02(j).

As stated above, Saenger fails to teach every limitation of the presently claimed invention. Fiordalice fails to overcome the deficiencies of the Saenger. Fiordalice discloses a method of forming monolithic interconnects in order to address the problem of cusping in large openings. The process includes forming an interconnect opening having two different widths in order to create a vertical plug 34 and a horizontal interconnect 36. (FIG. 5).

Applicants respectfully submit that the proposed combination fails to teach or suggest every limitation of independent claim 16. Neither Saenger nor Fiordalice teach or suggest a metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate and a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture flanking said conductive line. Instead, Saenger lacks any disclosure of a conductive line or a metal layer thereunder. Saenger merely discloses a conductive plug for transmitting a signal vertically. The aperture in Fiordalice includes two portions having two different widths, the bottom portion of the aperture, which defines a plug, does not appear to flank the top portion that contains the interconnect. Neither Saenger nor Fioradalice teaches or suggests a metal spacer abutting at least one sidewall of the aperture. Instead, Saenger teaches away from a metal spacer that extends the height of an aperture (Saenger, col. 4, lines 42-47) and Fiordalice lacks any disclosure of metal spacers. Thus, independent claim 16, from which claims 21 and 22 depend, is not obvious in view of the cited references.

The Federal Circuit has clearly indicated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *See, In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). The M.P.E.P. specifically upholds the finding of *In re Fine*, stating: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *See*, M.P.E.P. § 2143.03, (citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, as independent claim 16, from which claims 21 and 22 depend, is nonobvious in view of cited references, applicant submits that claims 21 and 22 are also nonobvious. Reconsideration of the rejection is respectfully requested.

Obviousness Rejection Based on U.S. Patent No. 5,701,647 to Saenger et al.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Saenger et al. (U.S. Patent No. 5,701,647). Applicant respectfully traverses this rejection, as hereinafter set forth.

As stated above, Saenger fails to teach or suggest every limitation of the presently claimed invention and lacks any teaching or suggestion to make the conductive line of the presently claimed invention. Further, the Federal Circuit has clearly indicated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *See, In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). The M.P.E.P. specifically upholds the finding of *In re Fine*, stating: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *See*, M.P.E.P. § 2143.03, (citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, as independent claim 16, from which claim 25 depends, is nonobvious in view of cited references, applicant submits that claim 25 is also nonobvious. Reconsideration of the rejection is respectfully requested.

New claims

New claims 100 through 129 have been added. Support for claim 100, which depends from claim 2, can be found in the specification and drawings, for example, page 6, lines 6-23 and FIGs. 1, 2, 3a and 3b. Claim 100 is distinguishable from the cited references for the same reasons indicated for independent claim 1. Further, applicant respectfully submits that claim 100 is allowable in view

of the primary reference Andricacos because Andricacos neither discloses, teaches or suggests a dielectric layer extending completely underneath a conductive line.

Support for claim 101, which depends from claim 16, can be found, for example, in FIGs. 4, 5, 6, 7a, 7b, 8 and 9. Claim 101 is distinguishable from the cited references for the same reasons indicated for independent claim 16.

Support for claim 102 can be found in the specification and drawings, for example, page 7, line 27 through page 12, line 5 and FIGs. 1, 2, 3a and 3b and dependent claim 2. Applicant submits that claim 103 is distinguishable from Andricacos for the same reasons as claim 1. Namely, Andricacos does not disclose a structure for transmitting a signal across a semiconductor device. Further, Andricacos lacks any disclosure of a conductive line.

Dependent claims 103 through 115 are substantially the same as dependent claims 3 through 15.

Support for claim 116 can be found in the specification and drawings, for example, page 12, line 6 through page 14, line 28 and FIGs. 4, 5, 6, 7a, 7b, 8 and 9. Applicant submits that claim 116 is distinguishable from Saenger for the same reasons as claim 16. Namely, Saenger does not disclose a structure for transmitting a signal across a substrate of a semiconductor device. Further, Saenger lacks any disclosure of a conductive line.

Dependent claims 117 through 129 are substantially the same as dependent claims 17 through 28 and 102.

Drawings

Applicant submits herewith corrected formal drawings, under cover of a separate Transmittal of Formal Drawings. Applicant respectfully requests approval of the corrected formal drawings.

CONCLUSION

Claims 1 through 28 and 100 through 129 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

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Enclosure: Version With Markings to Show Changes Made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A metallization structure for a semiconductor device, comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:

a metal layer defining a pattern on a portion of the substrate upper surface;

a conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said conducting layer having substantially aligned sidewalls; and

metal spacers flanking the sidewalls of the conducting layer and metal layer.

11. (Twice amended) The metallization structure of claim [11] 1, wherein the metal spacers are titanium or titanium nitride.

16. (Amended) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate [disposed thereon];

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture flanking said conductive line;

a metal spacer [on the] abutting at least one sidewall of said at least one sidewall of the aperture; and

a conductive layer substantially filling a remaining portion of the aperture.